**Lab # 10**

**OBJECTIVE:** To understand how a latch works to hold the data and set and reset states.

***NOTE:*** *Properly label the inputs and outputs in circuit diagrams & in timing diagrams*

**Lab Task 1:**

Implement the combinational circuit of **S'R' Latch** on **logic works** using **NAND gates** and make the **truth table.**

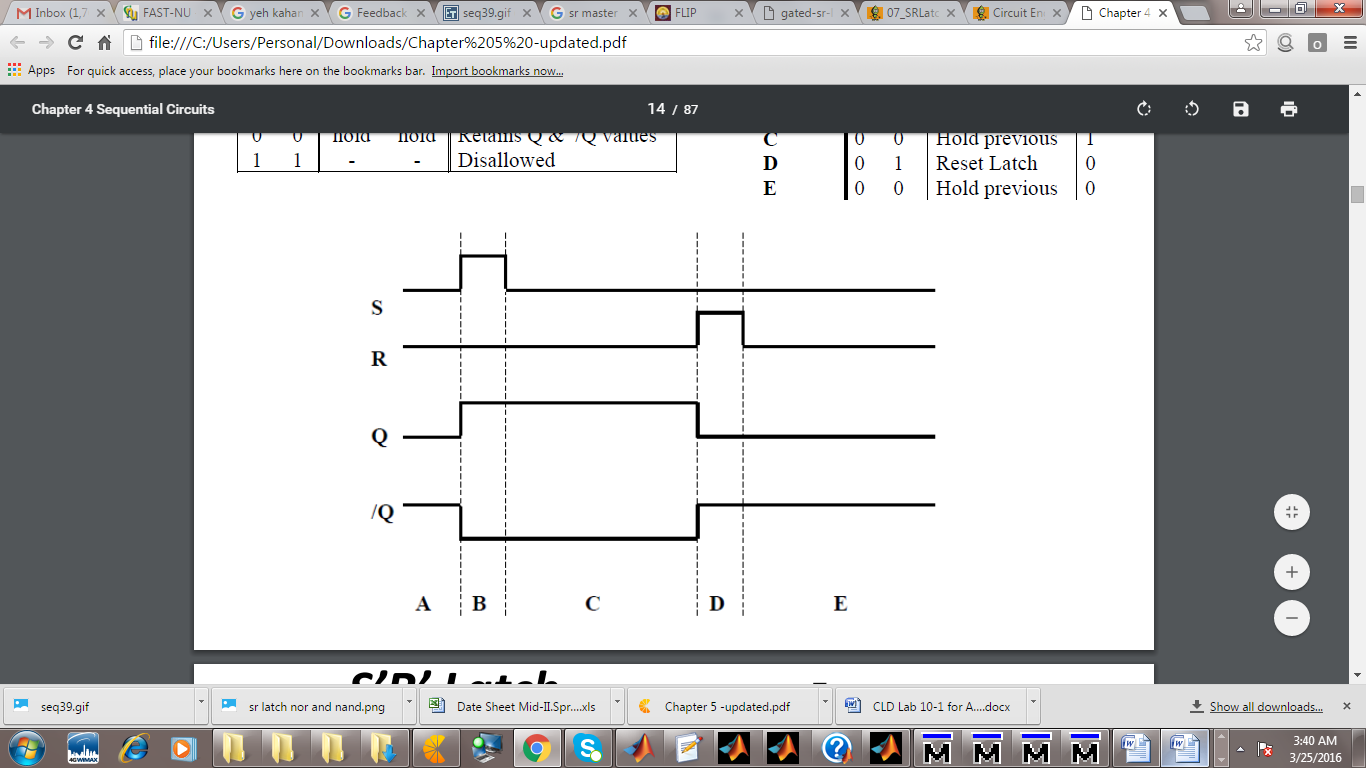
Show the **timing diagram** also on **logic works.**

**Lab Task 2:**

Implement the combinational circuit of **SR Latch** on **logic works** using **NOR** gates and make the **truth table**.

Show the **timing diagram** also on **logic works.**

**Timing Diagram:**

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**Lab Task 3:**

Implement the combinational circuit of **S'R' Latch** with **Control input** on **logic works** and make the **truth table.**

Show the **timing diagram** also on logic **works.**

**Timing Diagram:**

